



TITLE: DIFFERENTIAL SENSE LATCH SCHEME
INVENTORS NAME: Feng Chen et al.
SERIAL NO.: 09/606367

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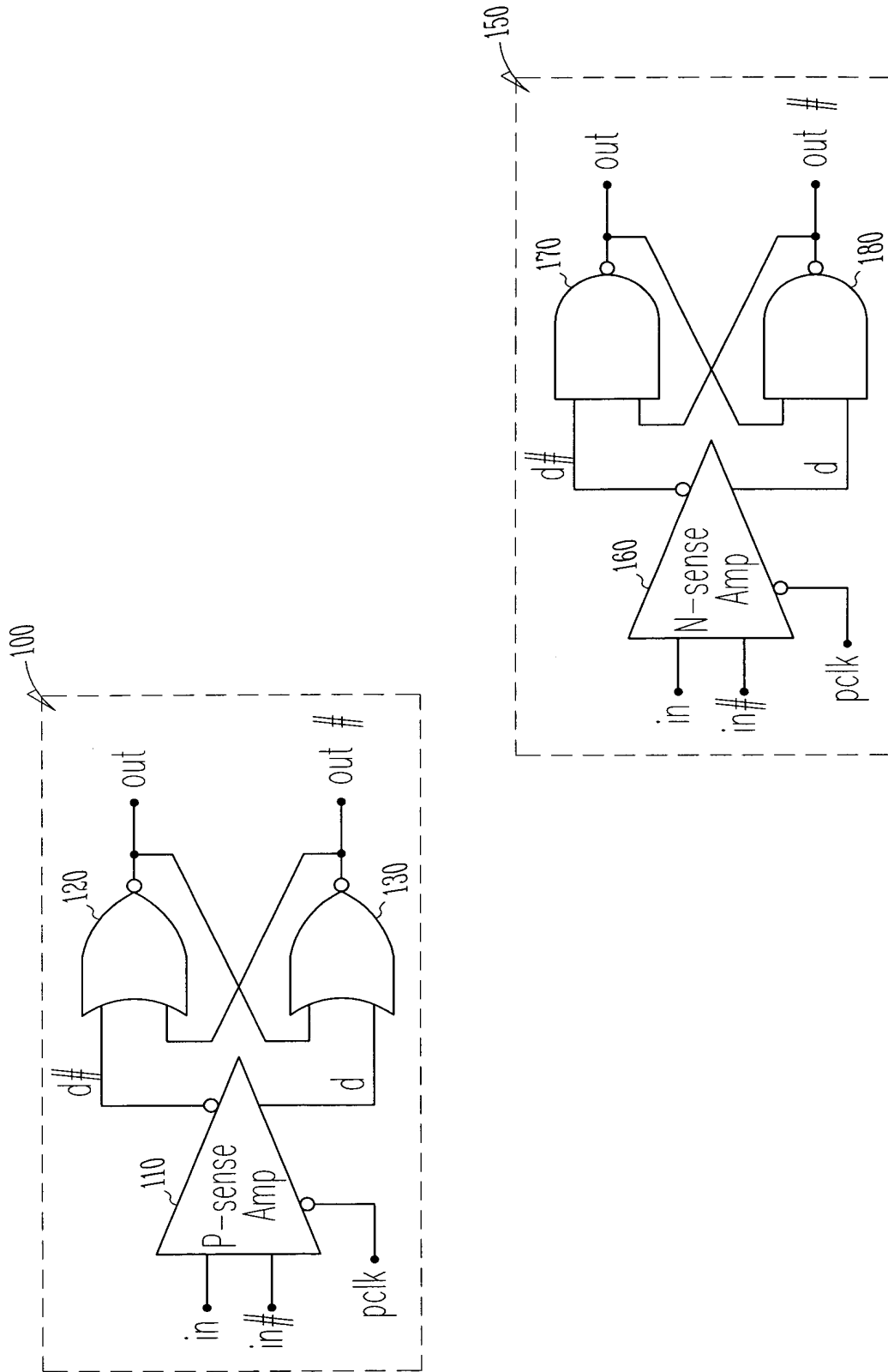


Fig. 1 (Prior Art)



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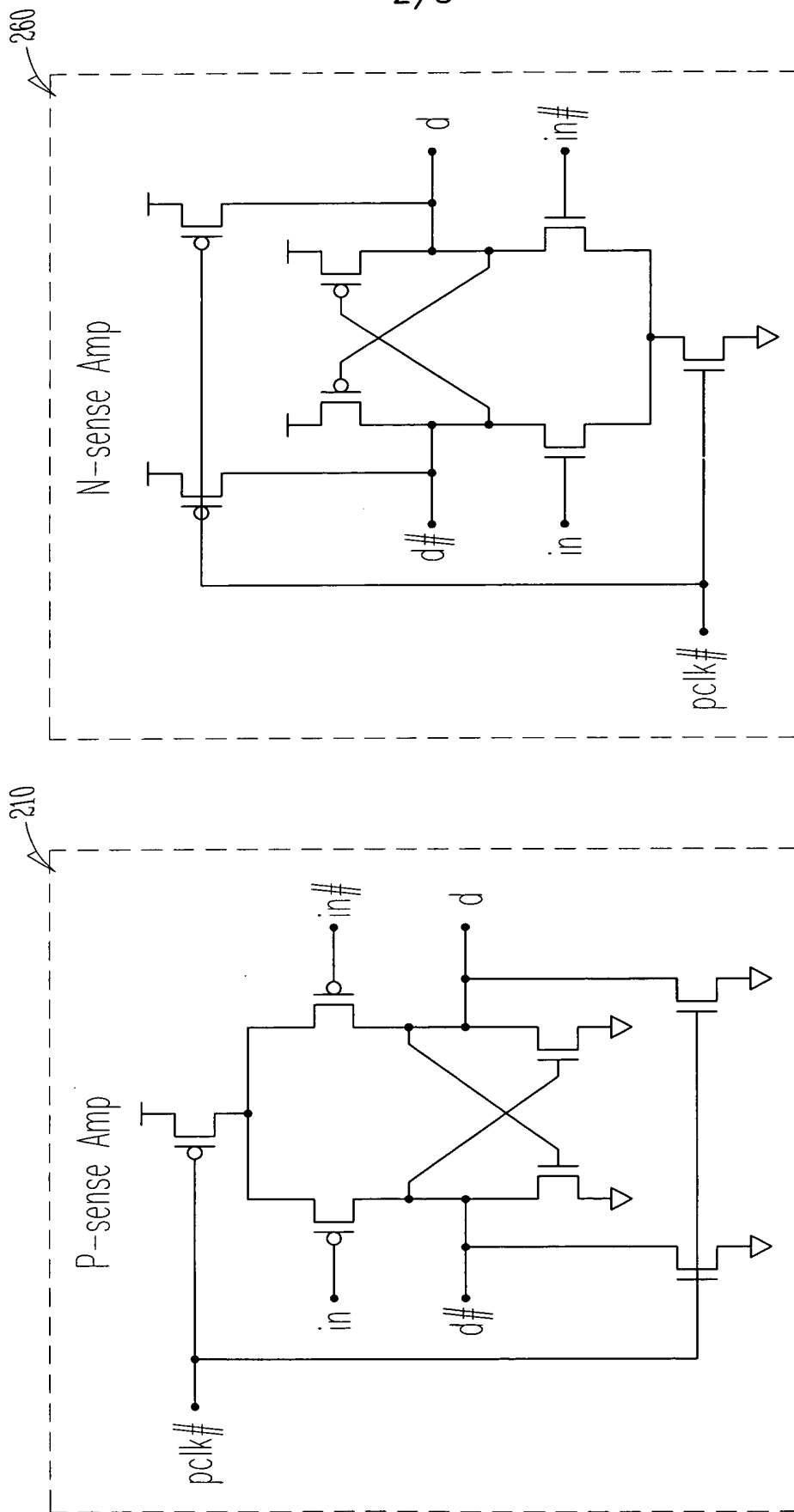


Fig. 2 (Prior Art)

The diagram illustrates a 2:1 multiplexer 300. It features two input sections, each enclosed in a dashed box labeled 'Keeper' (305). The first input section takes inputs 'cn' and 'bn' and produces output 'out'. The second input section takes inputs 'bn' and 'a' and produces output 'out#'. Both sections include a PMOS transistor (315, 375) and an NMOS transistor (320, 385) with a feedback loop. The circuit is divided into two main sections by a dashed line, with components labeled 310, 330, 340, 350, 360, 370, and 390. The clock signal 'pclk' is connected to the input of the first section. The output of the first section is 'out' and the output of the second section is 'out#'. The circuit is labeled 300 at the top left.



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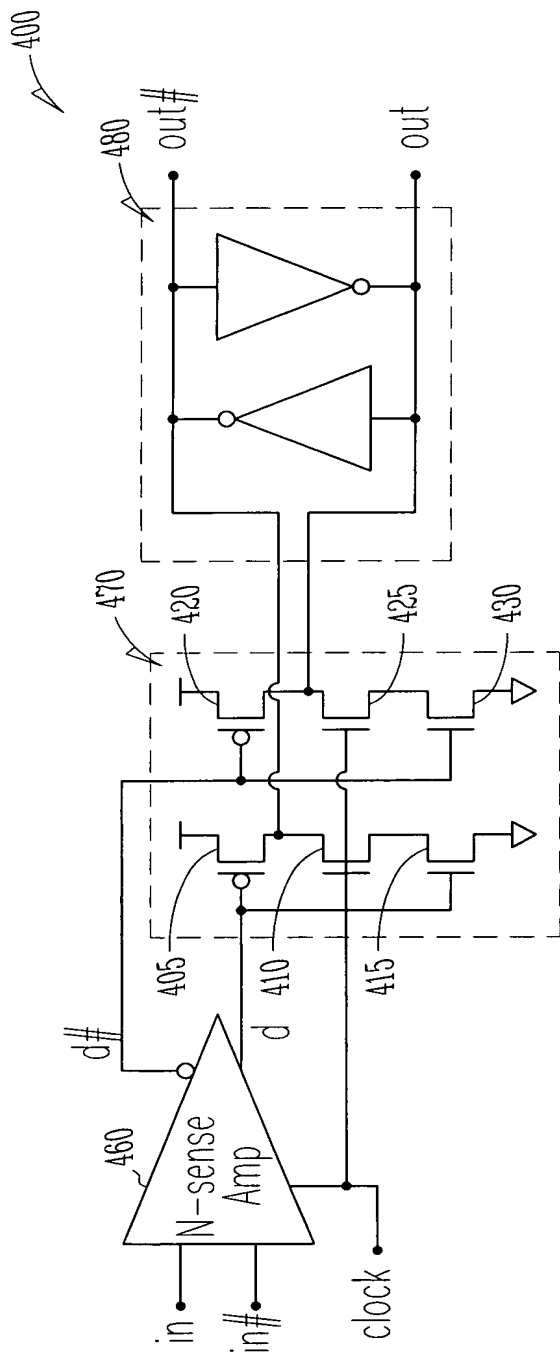


Fig. 4

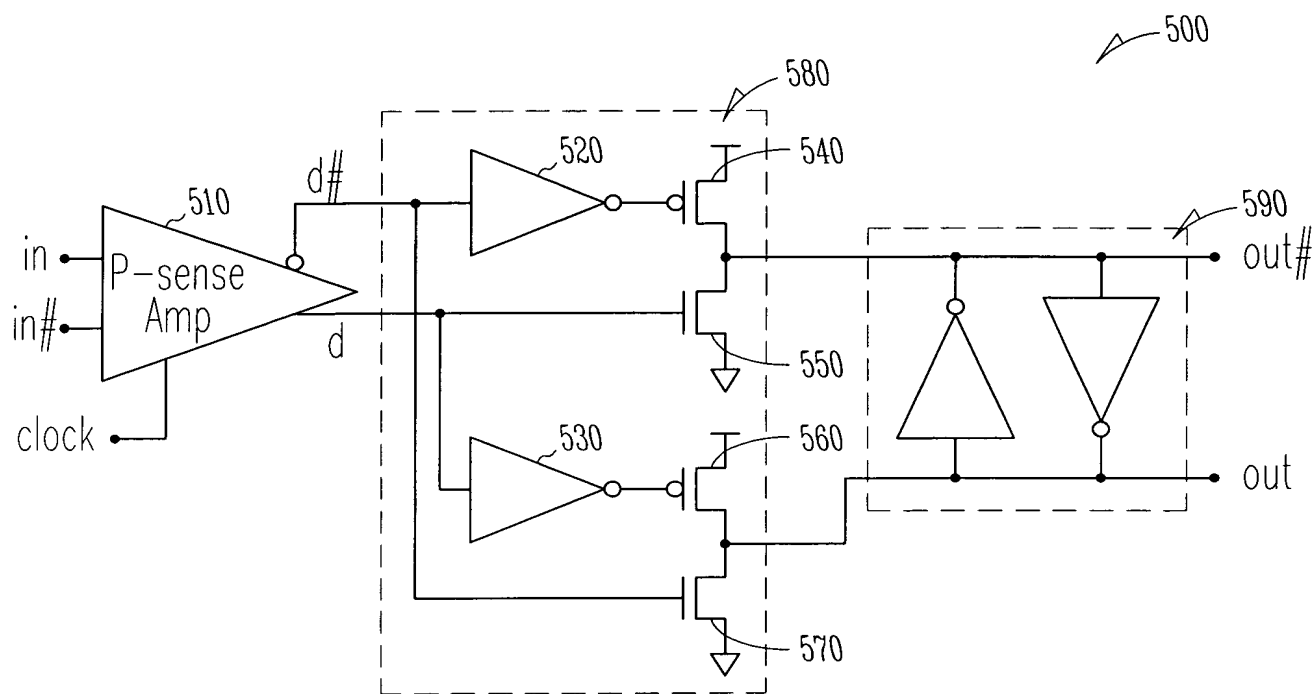


Fig. 5

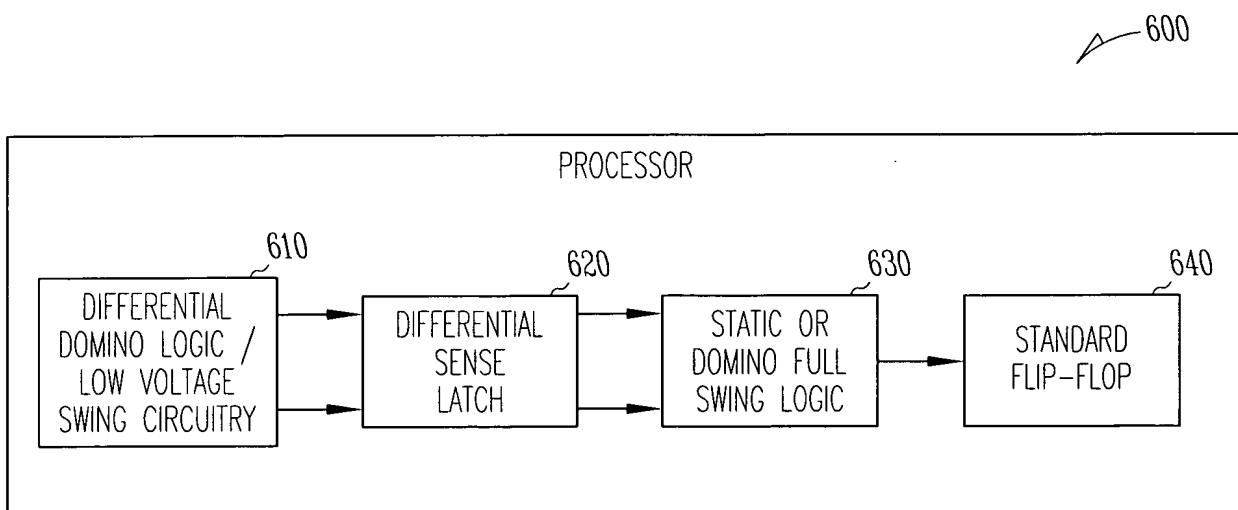


Fig. 6